Analog IC Design

Course Learning Objectives	• Study the basics of MOS Circuits. • Analyse the noise characteristics of amplifiers. • Study the performance parameters of amplifiers. • Comprehend the compensation techniques • Understand the detection and testing of faults
Course Outcomes	• Design amplifiers to meet user specifications. • Analyse the frequency and noise performance of amplifiers. • Design and analyse feedback amplifiers and one stage op amps. • Analyse stability of op amp. • Testing experience of logic circuits.

Unit 1: Single Stage Amplifiers

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

Unit 2: High Frequency and Noise Characteristics of Amplifiers

Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers

Unit 3: Feedback and Single Stage Operational Amplifiers

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-

stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

Unit 4: Stability, Frequency Compensation

Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two Stage Op Amps, Slewing in Two Stage Op Amps, Other Compensation Techniques.

Unit 5: Logic Circuit Testing

Faults in Logic Circuits- Basic Concepts of Fault Detection- Design for Testability- Ad Hoc Techniques, Level-Sensitive Scan Design, Partial Scan, Built-in Self-Test.

Course Duration: 45 Hours

Test Projects:

Use Cases:

PRACTICAL EXERCISE-1

1. Design a PMOS Device and analyze its I/V characteristics using EDA Tool

A. Design of Schematic and Simulation of IV curves PMOS Device Using EDA Tool

B. Design of Layout and Simulation of IV curves PMOS Device Using Electric EDA Tool

Task- [1 to 5]

Part A

- Explain the concept of PMOS Device in analog circuit design.
- Learn to create the schematic representation of PMOS Device using the Electric VLSI EDA Tool.
- Implement DRC to ensure the integrity and correctness of the PMOS Device design

◆ Simulate the PMOS Device to analyze its behavior and characteristics under different input conditions.

Part B

◆ Design the layout representation of a PMOS Device using Electric VLSI EDA tool.

◆ Perform DRC, ERC and LVS (Layout vs. Schematic) checks to ensure the

correctness and integrity of the PMOS Device layout.

◆ Conduct simulation on the layout of the PMOS Device to verify its characteristics under different input conditions.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

PRACTICAL EXERCISE-2

2. Design a NMOS Device and analyze its IV characteristics using EDA Tool

A. Design of Schematic and Simulation of NMOS Device Using EDA Tool

B. Design of Layout and Simulation of NMOS Device Using Electric EDA Tool Task-[1 to 5]

Part A

◆ Explain the concept of NMOS Device in analog circuit design.

◆ Learn to create the schematic representation of a NMOS Device using the Electric VLSI EDA Tool.

◆ Implement DRC to ensure the integrity and correctness of the NMOS Device design

◆ Simulate the NMOS Device to analyze its behavior and characteristics under different input conditions.

Part B

◆ Design the layout representation of NMOS Device using Electric VLSI EDA tool

◆ Perform DRC, ERC and LVS (Layout vs. Schematic) checks to ensure the correctness and integrity of the NMOS Device layout

◆ Conduct simulation on the layout of the NMOS Device to verify its characteristics under different input conditions.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

3. Design a CMOS inverter and analyze its characteristics using EDA Tool

A. Design of Schematic and Simulation of CMOS Inverter Using EDA Tool

B. Design of Layout and Simulation of CMOS Inverter Using Electric EDA Tool Task- [1 TO 5]

Part A

◆ Explain the concept of CMOS inverter in analog circuit design.

◆ Learn to create the schematic representation of a CMOS inverter using the Electric VLSI EDA Tool, capturing the NMOS and PMOS transistor connections.

◆ Implement DRC to ensure the integrity and correctness of the CMOS inverter design.

◆ Simulate the CMOS inverter to analyse its behavior and characteristics under different input conditions.

Part B

◆ Design the layout representation of a CMOS inverter using Electric VLSI EDA tool, considering the placement, and routing of NMOS and PMOS transistors.

◆ Perform DRC, ERC and LVS (Layout vs. Schematic) checks to ensure the correctness and integrity of the CMOS inverter layout.

◆ Conduct simulation on the layout of the CMOS inverter to verify its characteristics under different input conditions.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

4. Design a Common source amplifier and analyze its performance.

A. Design of Schematic and Simulation of Common source amplifier Using EDA Tool

B. Design of Layout and Simulation of Common source amplifier Using Electric EDA Tool

Task- [1 to 5]

Part A

◆ Explain the concept of a common-source amplifier and its importance in analog

circuit design.

◆ Design a schematic representation of the common-source amplifier in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the common-source amplifier schematic to evaluate its performance through waveform analysis.

◆ Learn the process of creating a layout representation for a common source amplifier using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of the Common Source Amplifier to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

5. Design a Common drain amplifier and analyze its performance.

A. Design of Schematic and Simulation of Common drain amplifier Using EDA Tool

B. Design of Layout and Simulation of Common drain amplifier Using Electric EDA Tool

Task- [1 to 5]

Part A

◆ Explain the concept of a common-drain amplifier and its importance in analog circuit design.

◆ Design a schematic representation of the common- drain amplifier in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the common- drain amplifier schematic to evaluate its performance through waveform analysis.

◆ Learn the process of creating a layout representation for a common drain amplifier using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of the Common drain Amplifier to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

6. Design a Common gate amplifier and analyze its performance.

A. Design of Schematic and Simulation of Common gate amplifier Using EDA Tool

B. Design of Layout and Simulation of Common gate amplifier Using Electric EDA Tool

Task-1 to 5

Part A

◆ Explain the concept of a common- gate amplifier and its importance in analog circuit design.

◆ Design a schematic representation of the common- gate amplifier in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the common- gate amplifier schematic to evaluate its performance through waveform analysis.

◆ Learn the process of creating a layout representation for a common gate amplifier using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of the Common gate Amplifier to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

7. Differential amplifier with PMOS current source load circuit

A. Design of Schematic and Simulation of Differential amplifier with PMOS current source load circuit Using EDA Tool

B. Design of Layout and Simulation of Differential amplifier with PMOS current source load circuit Using EDA Tool

Task-1 to 5

Part A

◆ Explain the concept of a Differential amplifier with PMOS current source load and its importance in analog circuit design.

◆ Design a schematic representation of Differential amplifier with PMOS current source load in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the differential amplifier schematic to evaluate its performance through waveform analysis.

◆ Learn the process of creating a layout representation for a Differential amplifier with PMOS current source load using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of the Differential amplifier with PMOS current source load to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

8. Design three stage ring oscillator circuit

A. Design of Schematic and Simulation of three stage ring oscillator Using EDA Tool

B. Design of Layout and Simulation of three stage ring oscillator Using Electric EDA Tool

Task-1 to 5

Part A

◆ Explain the concept of a three-stage ring oscillator and its importance in analog circuit design.

◆ Design a schematic representation of the three-stage ring oscillator in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the three-stage ring oscillator schematic to evaluate its performance through waveform analysis.

◆ Learn the process of creating a layout representation for three stage ring oscillators using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of the three-stage ring oscillator to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

9. Design five stage ring oscillator circuit

A. Design of Schematic and Simulation of five stage ring oscillator Using EDA Tool

B. Design of Layout and Simulation of five stage ring oscillator Using Electric EDA Tool

Task-1 to 5

Part A

◆ Explain the concept of a five-stage ring oscillator and its importance in analog circuit design.

◆ Design a schematic representation of five stage ring oscillator in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the five-stage ring oscillator schematic to evaluate its performance through waveform analysis.

Part-B

- Learn the process of creating a layout representation for five stage ring oscillators using the Electric VLSI EDA tool.
- Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.
- Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.
- Simulate the layout of five stage ring oscillator to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

10. Design CMOS Transmission Gate circuit

A. Design of Schematic and Simulation of CMOS Transmission Gate Using EDA Tool

B. Design of Layout and Simulation of CMOS Transmission Gate Using Electric EDA Tool

Task-1 to 5

Part A

- Explain the concept of CMOS Transmission Gate and its importance in analog circuit design.
- Design a schematic representation of CMOS Transmission Gate in the Electric VLSI EDA tool.
- Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.
- Simulate the CMOS Transmission Gate schematic to evaluate its performance through waveform analysis.

◆ Learn the process of creating a layout representation for CMOS Transmission Gate using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of CMOS Transmission Gate to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

11. Design Basic Current Mirror (MOSFET based) circuit.

A. Design of Schematic and Simulation of basic Current Mirror (MOSFET based) Using EDA Tool

B. Design of Layout and Simulation of basic Current Mirror Using Electric EDA Tool

Task-1 to 5

Part -A

◆ Explain the concept of basic Current Mirror and its importance in analog circuit design.

◆ Design a schematic representation of basic Current Mirror in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the basic Current Mirror schematic to evaluate its performance through waveform analysis.

◆ Learn the process of creating a layout representation for basic Current Mirror using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of basic Current Mirror to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

12. Design Cascode current mirror circuit

A. Design of Schematic and Simulation of Cascode current mirror Using EDA Tool

B. Design of Layout and Simulation of Cascode current mirror Using EDA Tool

Task - 1 to 5

Part - A

◆ Explain the concept of Cascode current mirror and its importance in analog circuit design.

◆ Design a schematic representation of Cascode current mirror in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the Cascode current mirror schematic to evaluate its performance through waveform analysis.

◆ Learn the process of creating a layout representation for Cascode current mirror using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of Cascode current mirror to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

13. Design Low voltage Cascode current mirror circuit

A. Design of Schematic and Simulation of Low voltage Cascode current mirror Using EDA Tool

B. Design of Layout and Simulation of Low voltage Cascode current mirror Using EDA Tool

Task-1 to 5

Part -A

◆ Explain the concept of Low voltage Cascode current mirror and its importance in analog circuit design.

◆ Design a schematic representation of Low voltage Cascode current mirror in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the Low voltage Cascode current mirror schematic to evaluate its performance through waveform analysis.

◆ Learn the process of creating a layout representation for Low voltage Cascode current mirror using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of Low voltage Cascode current mirror to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

14. Design Differential amplifier using OTA (Operational Transconductance Amplifier)

A. Design of Schematic and Simulation of Differential amplifier using OTA

Using EDA Tool

B. Design of layout and Simulation of Differential amplifier using OTA Using EDA Tool

Task-1 to 5

Part -A

◆ Explain the concept of Differential amplifier using OTA and its importance in analog circuit design.

◆ Design a schematic representation of Differential amplifier using OTA in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the Differential amplifier using OTA schematic to evaluate its performance through waveform analysis.

Part -B

◆ Learn the process of creating a layout representation for Differential amplifier using OTA using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of Differential amplifier using OTA to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

PRACTICAL EXERCISE-15

15 Design Three current-mirror OTA (Operational Transconductance Amplifier)

A. Design of Schematic and Simulation of Three current-mirror OTA Using EDA Tool

B. Design of Layout and Simulation of Three current-mirror OTA Using EDA Tool

Task-1 to 5 Part -A

◆ Explain the concept of Three current-mirror OTA and its importance in analog circuit design.

◆ Design a schematic representation of Three current-mirror OTA in the Electric VLSI EDA tool.

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations.

◆ Simulate the Three current-mirror OTA schematic to evaluate its performance through waveform analysis.

Part -B

◆ Learn the process of creating a layout representation for Three current-mirror OTA using the Electric VLSI EDA tool.

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns.

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking.

◆ Simulate the layout of Three current-mirror OTA to analyze its performance and characteristics.

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence

PRACTICAL EXERCISE-16

16 Design Two Stage Miller OTA (Operational Transconductance Amplifier)

A. Design of Schematic and Simulation of Two Stage Miller OTA Using EDA Tool

B. Design of Layout and Simulation of Two Stage Miller OTA Using EDA Tool

Task-1 to 5 Part -A

◆ Explain the concept of Two Stage Miller OTA and its importance in analog circuit design

◆ Design a schematic representation of Two Stage Miller OTA in the Electric VLSI EDA tool

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations

◆ Simulate the Two Stage Miller OTA schematic to evaluate its performance through waveform analysis

Part -B

◆ Learn the process of creating a layout representation for Two Stage Miller OTA using the Electric VLSI EDA tool

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking

◆ Simulate the layout of Two Stage Miller OTA to analyze its performance and characteristics

Software Tools: Electric VLSI EDA Tool- Open Source Equivalent EDA tool to Cadence

17. Design Inverting amplifier with current-mirror load

A. Design of Schematic and Simulation of Inverting amplifier with current- mirror load Using EDA Tool

B. Design of Layout and Simulation of Inverting amplifier with current-mirror load Using EDA Tool

Task-1 to 5

Part -A

◆ Explain the concept of Inverting amplifier with current-mirror load and its importance in analog circuit design

◆ Design a schematic representation of Inverting amplifier with current-mirror load in the Electric VLSI EDA tool

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations

◆ Simulate the Inverting amplifier with current-mirror load schematic to evaluate its performance through waveform analysis

Part -B

◆ Learn the process of creating a layout representation for Inverting amplifier with current-mirror load using the Electric VLSI EDA tool

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking

◆ Simulate the layout of Inverting amplifier with current-mirror load to analyze its performance and characteristics

Software Tools: Electric VLSI EDA Tool- Open Source Equivalent EDA tool to Cadence

18. Design of two stage opomp consisting of differential pair, common source stage and a current mirror

A. Design of Schematic and Simulation of two stage opamp consisting of differential pair, common source stage and a current mirror Using EDA Tool

B. Design of Layout and Simulation of two stage opamp consisting of differential pair, common source stage and a current mirror Using EDA Tool

Task-1 to 5

Part -A

◆ Explain the concept of two stage opamp consisting of differential pair, common source stage and a current mirror nd its importance in analog circuit design

◆ Design a schematic representation of two stage opamp consisting of differential pair, common source stage and a current mirror in the Electric VLSI EDA tool

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations

◆ Simulate the two stage opamp consisting of differential pair, common source stage and a current mirror schematic to evaluate its performance through waveform analysis

Part -B

◆ Learn the process of creating a layout representation for two stage opamp consisting of differential pair, common source stage and a current mirror using the

Electric VLSI EDA tool

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns

◆ -Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking

◆ Simulate the layout of two stage opamp consisting of differential pair, common source stage and a current mirror to analyze its performance and characteristics

Software Tools: Electric VLSI EDA Tool- Open Source Equivalent EDA tool to Cadence

19. Design of Triple Casocode CS Amplifier with current source load

A. Design of Schematic and Simulation of Triple Casocde CS Amplifier with current source load Using EDA Tool

B. Design of Layout and Simulation of Triple Casocde CS Amplifier with current source load Using EDA Tool

Task-1 to 5

Part -A

◆ Explain the concept of Triple Casocde CS Amplifier with current source load and

its importance in analog circuit design

◆ Design a schematic representation of Triple Casocde CS Amplifier with current source load in the Electric VLSI EDA tool

◆ Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations

◆ Simulate the Triple Casocde CS Amplifier with current source load

Part -B

◆ Learn the process of creating a layout representation for Triple Casocde CS Amplifier using the Electric VLSI EDA tool

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking

◆ Simulate the layout of Triple Casocde CS Amplifier to analyze its performance and characteristics

Software Tools: Electric VLSI EDA Tool- Open Source Equivalent EDA tool to Cadence

PRACTICAL EXERCISE-20

20. Design of two single-ended differential amplifiers. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror

A. Design of Schematic and Simulation of two single-ended differential amplifiers. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror Using EDA Tool

B. Design of Layout and Simulation of two single-ended differential amplifiers. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror Using EDA Tool

Task-1 to 5

Part -A

- Explain the concept of Design of the design of two single-ended differential amplifiers. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror and its importance in analog circuit design
- Design a schematic representation of Design of the design of two single-ended differential amplifiers. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror in the Electric VLSI EDA tool
- Perform the design verification checks such as DRC and ERC to verify the integrity of the schematic design and identify any potential errors or violations

Simulate the Design of the design of two single-ended differential amplifiers. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror

Part -B

◆ Learn the process of creating a layout representation of two single-ended differential amplifiers. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror using the Electric VLSI EDA tool

◆ Perform DRC and ERC to ensure that the layout meets the specified design rules and to address any potential electrical connectivity concerns

◆ Verify the layout's connectivity and compatibility through Layout vs. Schematic (LVS) checking

◆ Simulate the layout of two single-ended differential amplifiers. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror to analyze its performance and characteristics

Software Tools: Electric VLSI EDA Tool- Open-Source Equivalent EDA tool to Cadence